

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Canceled)

2. (Currently Amended) A latch circuit receiving an inverting input signal, a non-inverting clock signal, an inverting clock signal, and a common mode control signal; and producing a non-inverting output signal and an inverting output signal, as claimed in claim 1 comprising transistors, each transistor comprising a source, a gate and a drain, the latch circuit further comprising;

[[ -]] a first pair of transistors comprising a first transistor and a second transistor having their sources having its drain coupled to the non-inverting output signal and its gate coupled to the inverting output signal each other;

[[ -]] a second pair of transistors comprising a third transistor and a fourth transistor having its drain their sources coupled to the non-inverting output signal, its gate coupled to the non-inverting clock signal, and its source coupled to the source of the first transistor each other;

[[ -]] a third gate of the second transistor having its gate being coupled to the common mode control signal, a gate of the third transistor and further its source coupled to the source of the first transistor; control signal;

[[ -]] a fourth positive feedback from the non-inverting output to a gate of the first transistor, having its drain coupled to the drain of the third transistor, and its gate coupled to the common mode control signal;

[[ -]] a fifth transistor pair of switches comprising a first switch and a second switch having its their respective drains and sources coupled to the non-inverting output signal, its gate coupled to respective drains and sources of the inverting input signal, first transistor and its source coupled to the source of the fourth transistor; respectively, and

[[ -]] a sixth transistor having its drain coupled to the non-inverting output signal, its gate of coupled to the first switch being driven by the inverting clock signal and gate of the second switch being driven by the non-inverting clock signal its source coupled to the source of the fourth transistor.

3. (Currently Amended) The A-latch as claimed in claim 2, wherein

[[ -]] the sources of the first transistor, and the second transistor, and the third transistor are coupled to supplied by a first current source, and

[[ -]] the sources of the fourth third-transistor, and the fifth fourth-transistor, and the sixth transistor are coupled supplied by to a second current source.

4. (Currently Amended) The A-latch circuit as claimed in claim 3, wherein the first current source and the second current source provide substantially equal currents.

5. (Currently Amended) The A-latch circuit as claimed in claim ~~23~~, wherein the non-inverting output is drain of the first transistor and the drain of the fourth transistor are coupled to each other and further coupled to a supply voltage via a first resistor means.

6. (Currently Amended) The A-latch circuit as claimed in claim 2, wherein the inverting output is drain of the second transistor is coupled to a drain of the third transistor, the drains being further coupled to the supply voltage via a second resistor means.

7. (Currently Amended) The A-latch circuit as claimed in claim ~~26~~, wherein the second resistor ~~means~~ is coupled to a ~~reference terminal via a third current source.~~

8. (Currently Amended) The A-latch circuit as claimed in ~~any of the preceding claim 1 3,~~ wherein the first current source and the second current source comprises a series connection of a main current channel of a controlled current source and a third resistor means.

9. (Currently Amended) The A-latch circuit as claimed in claim 8, wherein the controlled sources ~~current source~~ are is controlled by a voltage.

10. (Currently Amended) A latch circuit as claimed in claim 1, adapted for differential input signals, and comprising:

\_\_\_\_\_ a first latch portion and a second latch portion, which are substantially identical, each latch portion comprising:

[[ - ]] a differential input with an inverting input and a non-inverting input;

[[ - ]] a differential output with an inverting output and a non-inverting output; and

\_\_\_\_\_ a control input which determines a threshold for the input signals such that when the input signal is a larger than the threshold the output latch is in a HIGH logic state and in a LOW state when the signal is smaller than the threshold, wherein

[[ - ]] one of the outputs of the first latch portion being is coupled to one of the inputs of the second latch portion having opposite polarity; of the second latch portion,

[[ - ]] one of the outputs of the second latch portion being is coupled to one of the inputs of the first latch portion having opposite polarity; of the first latch portion,; and

[[ - ]] a differential input signal being provided at to the latch circuit is coupled to one of the inputs of the first latch portion and to one of the inputs of the second latch portion having an opposite polarity; of the second latch portion, respectively, and

[[ - ]] each of the latch portions comprising a control input which is coupled a respective control signal, which determines a threshold for the input signal such that if the input signal is at larger than the threshold the output latch is in a HIGH logic state and in a LOW state if the signal is smaller than the threshold, respectively.

11. (Currently Amended) The A-latch circuit as claimed in claim 10 comprising transistors, each transistor comprising a source, a gate and a drain, and wherein each latch portion further comprises:

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[[~~-~~]] a first ~~pair of transistors comprising a first transistor and a second transistor~~ having their ~~sources~~its drain coupled ~~each other, respectively to the non-inverting output of the latch portion~~ and its gate coupled to the non-inverting input of the latch portion;

[[~~-~~]] a second ~~pair of transistors comprising a third~~ having its drain coupled to the non-inverting output signal of the latch portion, its gate coupled to a non-inverting clock signal, and its source coupled to the source of the first transistor; ~~and a fourth transistor having their sources coupled each other, respectively~~

[[~~-~~]] a ~~gate of the second~~ third transistor being coupled to a ~~having its gate of the third transistor respectively and further coupled to~~ the control input and its source coupled to the source of the first transistor; ~~a DC voltage level;~~

[[~~-~~]] a ~~fourth pair of switches comprising a first switch and a second switch, the switches including transistors~~ having their respective ~~its drains and sources coupled to the respective drains and sources of the~~ third first-transistor and its gate coupled to the control input; ~~the fourth transistor, respectively;~~

[[~~-~~]] ~~gate of the first switch being driven by a binary clock signal and gate of the second switch being driven by an inverted binary clock signal,~~ a fifth transistor having its drain coupled to the non-inverting output of the latch portion, its gate coupled to the inverting input of the latch portion, and its source coupled to the source of the fourth transistor; and

[[~~-~~]] ~~a sixth~~ the two latch portions being crossed coupled such that a gate of the first transistor of a portion is having its drain coupled to the respective non-inverting output of the other portion, respectively latch portion, its gate coupled to an inverting clock signal, and its source coupled to the source of the fourth transistor.

12. (Currently Amended) ~~The A-latch~~ as claimed in claim ~~Claim~~ 11 wherein

[[~~-~~]] the sources of the first transistor; ~~and the second transistor, and the third transistor~~ are ~~supplied by~~ coupled to a first current source; ~~and~~

[[~~-~~]] the sources of the ~~third~~ fourth transistor, the fifth transistor, and the ~~fourth~~ sixth transistor are coupled to ~~supplied by~~ a second current source.

13. (Currently Amended) The A-latch circuit as claimed in claim 12, wherein the first current source and the second current source provide substantially equal currents.

14. (Currently Amended) The A-latch circuit as claimed in claim 1011, wherein each latch portion further comprises a the drain of the first resistor coupling the inverting output transistor and the drain of the latch portion fourth transistor are coupled to each other respectively and further coupled to a supply voltage via a first resistor means.

15. (Currently Amended) The A-latch circuit as claimed in claim 1014, wherein each latch portion further comprises the drain of the a second resistor coupling the non inverting output transistor is coupled to a drain of the third transistor, respectively the drains being further coupled latch portion to the supply voltage via a second resistor means.

16. (Currently Amended) The A-latch circuit as claimed in claim 1012, wherein the first current source (10) and the second current source comprises a series connection of a main current channel of a controlled current source and a third resistor means.

17. (Currently Amended) The A-latch circuit as claimed in claim 16, wherein the controlled current sources are is controlled by a voltage.